Zaamo and Zalrsc Extensions

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Preamble

This document is in the Ratified state

No changes are allowed. Any desired or needed changes can be the subject of a follow-on new extension. Ratified extensions are never revised.

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Contributors

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Chapter 1. Atomic Memory Operations Extension (Zaamo)

The Zaamo extension comprises the atomic memory operation (AMO) subset of the A extension [1].

For RV32, the Zaamo extension includes the following instructions:

- `AMOSWAP.W`
- `AMOADD.W`
- `AMOAND.W`
- `AMOOR.W`
- `AMOXOR.W`
- `AMOMAX[U].W`
- `AMOMIN[U].W`

For RV64, the Zaamo extension includes the following instructions:

- `AMOSWAP.W/D`
- `AMOADD.W/D`
- `AMOAND.W/D`
- `AMOOR.W/D`
- `AMOXOR.W/D`
- `AMOMAX[U].W/D`
- `AMOMIN[U].W/D`

The Zacas extension [2] depends on the Zaamo extension.

The Zaamo extension enables microcontroller class implementations to utilize atomic primitives from the AMO subset of the A extension. Typically such implementations do not have caches and thus may not be able to naturally support the `LR`/`SC` instructions provided by the A extension.

Chapter 2. Load-Reserved/Store-conditional Extension (Zalrsc)

The Zalrsc extension comprises the Load-Reserved/Store-Conditional instruction subset of the A extension.

For RV32, the Zalrsc extension includes the `LR.W` and `SC.W` instructions.

For RV64, the Zalrsc extension includes the `LR.W/D` and `SC.W/D` instructions.

The fetch-and-op style atomic primitives provided by the A extension support better scaling for highly parallel systems. Simpler implementations that do not have such scaling requirements may implement the Zalrsc subset of the A extension to support atomic primitives.

Bibliography

[1] “RISC-V Instruction Set Manual, Volume I: Unprivileged ISA .” [Online]. Available: github.com/riscv/riscv-isa-manual.

[2] “Atomic Compare-and-Swap (CAS) instructions.” [Online]. Available: github.com/riscv/riscv-zacas.