The V extension supports all vector integer single-width and widening reduction operations (Sections Vector Single-Width Integer Reduction Instructions, Vector Widening Integer Reduction Instructions).

The V extension supports all vector mask instructions (Section Vector Mask Instructions).

The V extension supports all vector permutation instructions (Section Vector Permutation Instructions).

The V extension depends upon the F and D extensions, and implements all vector floating-point instructions (Section Vector Floating-Point Instructions) for floating-point operands with EEW=32 or EEW=64 (including widening instructions and conversions between FP32 and FP64). Vector single-width floating-point reductions (Vector Single-Width Floating-Point Reduction Instructions) for EEW=32 and EEW=64 are supported as well as widening reductions from FP32 to FP64.

Note

As is the case with other RISC-V extensions, it is valid to include overlapping extensions in the same ISA string. For example, RV64GCV and RV64GCV_Zve64f are both valid and equivalent ISA strings, as is RV64GCV_Zve64f_Zve32x_Zvl128b.

18.4. Zvfhmin: Vector Extension for Minimal Half-Precision Floating-Point

The Zvfhmin extension provides minimal support for vectors of IEEE 754-2008 binary16 values, adding conversions to and from binary32. When the Zvfhmin extension is implemented, the `vfwcvt.f.f.v` and `vfncvt.f.f.w` instructions become defined when SEW=16. The EEW=16 floating-point operands of these instructions use the binary16 format.

The Zvfhmin extension depends on the Zve32f extension.

18.5. Zvfh: Vector Extension for Half-Precision Floating-Point

The Zvfh extension provides support for vectors of IEEE 754-2008 binary16 values. When the Zvfh extension is implemented, all instructions in Sections Vector Floating-Point Instructions, Vector Single-Width Floating-Point Reduction Instructions, Vector Widening Floating-Point Reduction Instructions, Vector Floating-Point Move Instruction, Vector Floating-Point Slide1up Instruction, and Vector Floating-Point Slide1down Instruction become defined when SEW=16. The EEW=16 floating-point operands of these instructions use the binary16 format.

Additionally, conversions between 8-bit integers and binary16 values are provided. The floating-point-to-integer narrowing conversions (`vfncvt[.rtz].x[u].f.w`) and integer-to-floating-point widening conversions (`vfwcvt.f.x[u].v`) become defined when SEW=8.

The Zvfh extension depends on the Zve32f and Zfhmin extensions.

Note

Requiring basic scalar half-precision support makes Zvfh's vector-scalar instructions substantially more useful. We considered requiring more complete scalar half-precision support, but we reasoned that, for many half-precision vector workloads, performing the scalar computation in single-precision will suffice.