



RISC-V Quality of Service Controllers Table (RQSC) ACPI Specification

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Preamble



This document is in the [Frozen state](#)

Assume everything can change. This draft specification will change before being accepted as standard, so implementations made to this draft specification will likely not conform to the future standard.

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Chapter 1. Introduction

This document describes the specification for the ACPI [1] description of the RISC-V Quality of Service Controller Register Interfaces for OSPM level configuration and control of Quality of Service features.

1.1. Terminology

Term	Description
ACPI	Advanced Configuration and Power Interface
CBQRI	Capacity and Bandwidth Controller QoS Register Interface
HMAT	Hardware Memory Affinity Table
MCID	Monitoring Counter Identifier
NUMA	Non-Uniform Memory Access
OSPM	Operating System Power Manager
PPTT	Processor Properties Topology Table
QoS	Quality of Service
RCID	Resource Control Identifier
RISC	Reduced Instruction Set Computer
RQSC	RISC-V Quality of Service Controller
SRAT	System Resource Affinity Table
UMA	Uniform Memory Access

Chapter 2. The ACPI RQSC Table

The Capacity and Bandwidth QoS controllers in a system are described by the ACPI RQSC table. The actual register interface is specified in the RISC-V Capacity and Bandwidth Controller QoS Register Interface specification [2].

The RQSC table describes the properties of the QoS controllers in the system and the resources managed by the each of the QoS controllers. The RQSC table does not describe any topological arrangement of QoS controllers but such topological arrangement may be inferred, when applicable, by determining the topological arrangement of the resources managed by the QoS controller using the ACPI tables that describe the property of those resources.

The capacity or bandwidth controller behavior for handling a request with a non-zero RCID value before configuring the capacity or bandwidth controller respectively with capacity or bandwidth allocation for that RCID is UNSPECIFIED. Software must ensure that the QoS controllers accessed by a request with non-zero RCID values are configured appropriately prior to initiating such requests.

The following diagram illustrates the various components of the RQSC table. The RQSC table contains among other typical ACPI table fields, the count and the list of QoS Controller Structures. Each QoS Controller Structure describes the properties of a QoS Controller and contains one or more Resource Structures. Usually, a QoS controller is associated with a single Resource structure. However, in some implementations, a QoS controller may be associated with multiple Resource structures. Each Resource Structure provides an ACPI locator for the resource governed by that QoS controller.

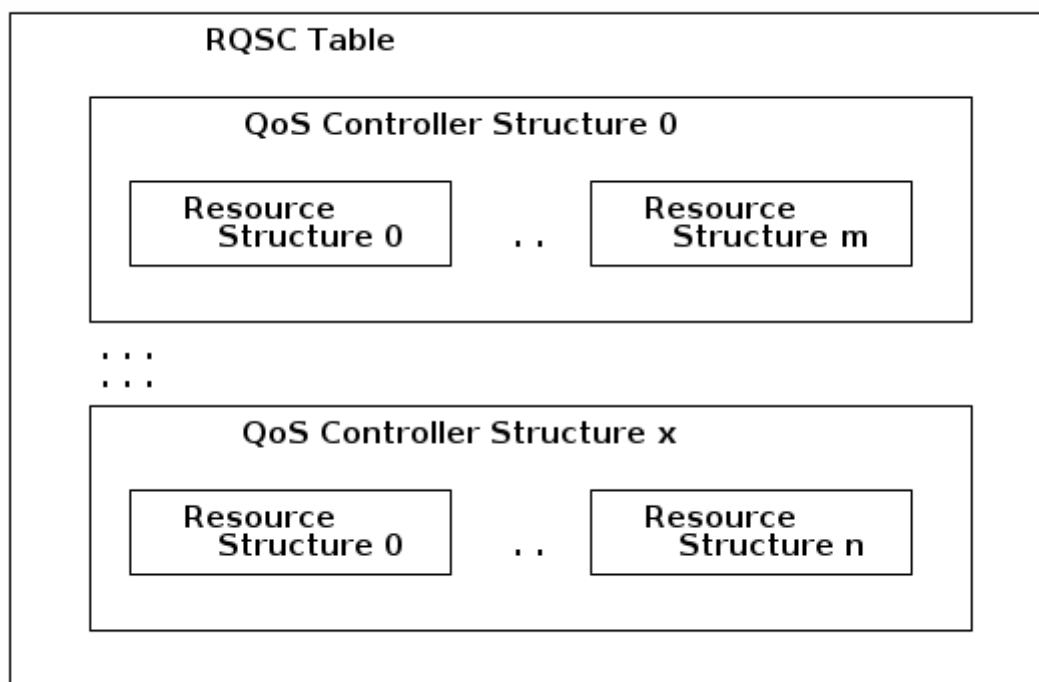


Figure 1. RQSC Table Components



The RQSC table presents controllers as a flat set and does not directly encode hierarchy. Any hierarchy present in the implementation is conveyed through the association of controllers with resources described elsewhere. For example, if an SoC implements Cache Capacity controllers for both an L2 cache within a core or cluster of cores and a last-level

cache (LLC), the hierarchy is captured by the resource associations of those controllers, as indicated by the Cache ID fields in the corresponding PPTT descriptions.

The structure of the RQSC is described in [Table 1](#).

Table 1. The RQSC Table

Field	Byte Length	Byte Offset	Description
Header			
- Signature	4	0	'RQSC'. RISC-V Quality of Service Controllers Table.
- Length	4	4	Length of the entire RQSC table in bytes.
- Revision	1	8	Revision number. Current Value: 1
- Checksum	1	9	Entire table must sum to zero
- OEMID	6	10	OEM ID
- OEM Table ID	8	16	For RQSC Table, the table ID is the manufacturer model ID
- OEM Revision	4	24	OEM revision of RQSC Table for supplied OEM Table ID
- Creator ID	4	28	Vendor ID of utility that created the table
- Creator Revision	4	32	Revision of utility that created the table
Body			
- Number of QoS Controllers	4	36	The number of system level QoS controller structures that immediately follow.
- QoS Controller Structure [n]	-	40	List of Quality of Service Controller Structures. See Table 2 table below.

Table 2. Quality of Service Controller Structure

Field	Byte Length	Byte Offset	Description
Header			
- Controller Type	1	0	Identifies the register interface supported by this controller, as defined by the RISC-V CBQRI Specification. <ul style="list-style-type: none"> • 0 - Capacity • 1 - Bandwidth • 2-0x7F - Reserved for future standard use • 0x80-0xFF - Designated for Vendor specific use
- Reserved	1	1	Reserved. Must be 0
- Length	2	2	Length of the Quality of Service Controller structure in bytes. The Length includes all resource structures for this controller.

Field	Byte Length	Byte Offset	Description
- Register Interface Address	12	4	Contains the processor-relative base address, represented in Generic Address Structure (GAS) format, of the controller's register space.
- RCID Count	2	16	<p>A non-zero value indicates that the controller supports allocation capability and specifies the number of Resource Control IDs (RCIDs) supported by the controller. A value of zero indicates that no allocation control is available.</p> <p>OSPM must use the RCID Count field to determine the number of RCIDs supported by the controller, regardless of any count reported by the hardware.</p>
- MCID Count	2	18	<p>A non-zero value indicates that the controller supports monitoring capability and specifies the number of Monitoring Control IDs (MCIDs) supported by the controller. A value of zero indicates that no monitoring control is available.</p> <p>OSPM must use the MCID Count field to determine the number of MCIDs supported by the controller, regardless of any count reported by the hardware.</p> <p>At least one of RCID Count or MCID Count must be non-zero.</p>
- Controller Flags	2	20	Controller-Specific flags. Refer to Table 3 for details.
- Number of Resources	2	22	Number of Resource structures associated with this QoS controller.
- Resource Structure [n]	-	24	List of Resource Structures associated with this QoS controller.

Table 3. Controller Flags

Bit	Description
0	When set, indicates the controller supports allocating zero capacity blocks or zero bandwidth blocks to an RCID.
1-7	Reserved for future standard use.
8-15	Designated for Vendor specific use.

Table 4. Resource Structure

Field	Byte Length	Byte Offset	Description
Header			
- Resource Type	1	0	<ul style="list-style-type: none"> • 0 - Cache • 1 - Memory • 2 - 0x7F - Reserved for future standard use • 0x80 - 0xFF - Designated for Vendor specific use
- Reserved	1	1	Reserved. Must be 0
- Length	2	2	Length of this Resource Structure, in bytes. The length includes the Resource-Specific Data bytes. A value of 20 indicates that no Resource-Specific Data is present.
- Resource Flags	2	4	Resource Type Specific flags. Refer to Table 5 for details.
- Reserved	1	6	Reserved. Must be 0
- Resource ID Type	1	7	<p>Type of the Resource ID described by Resource ID 1 and Resource ID 2 fields.</p> <ul style="list-style-type: none"> • 0 - Processor Cache • 1 - Memory Range • 2 - Memory-Side Cache • 3 - ACPI Device: Used in cases where the resource is described as an ACPI device in a platform specific or vendor specific implementation. • 4 - PCI Device: Used in cases where the resource is a PCI device in a platform specific or vendor specific implementation. For example, a network interface card implementing ethernet ports. • 5 - 0x7F - Reserved for future standard use • 0x80 - 0xFF - Designated for Vendor specific use

Field	Byte Length	Byte Offset	Description
- Resource ID 1	8	8	Primary identifier for the resource. The interpretation of this field depends on the Resource ID Type. For example, this may contain a Cache ID, Proximity Domain, or device identifier depending on the resource type. Refer to Table 6 for type-specific details.
- Resource ID 2	4	16	Auxiliary identifier for the resource. Some resource types require additional information beyond Resource ID 1 to uniquely identify the resource. For example, ACPI devices may share the same Hardware ID (_HID) and require a Unique ID (_UID) to distinguish them. Refer to Table 7 for type-specific details. Reserved when not required by the resource type.
- Resource Specific Data	-	20	Depends on the Resource Type Field. Refer to Table 8 for details.

Table 5. Resource Flags

Bit	Description
All Other Resource Types	
0-7	Reserved for future standard use.
8-15	Designated for Vendor specific use.

Table 6. Resource ID 1


Field	Byte Length	Byte Offset	Description
Resource ID Type [0 - Processor Cache]			
Cache ID	4	0	Unique Cache ID from the PPTT table's Cache Type Structure (Table 5.159 in ACPI Specification 6.5) that this controller is associated with.
Reserved	4	4	Reserved.
Resource ID Type [1 - Memory Affinity Structure]			
Proximity Domain	4	0	Proximity domain from the SRAT table's Memory Affinity Structure the resource is associated with. If the SRAT table is not implemented, then this value shall be 0 indicating a UMA memory configuration.
Reserved	4	4	Reserved.
Resource ID Type [2 - Memory-Side Cache]			

Field	Byte Length	Byte Offset	Description
Proximity Domain	4	0	Proximity domain from the SRAT table's Memory Affinity Structure the resource is associated with. If the SRAT table is not implemented, then this value shall be 0 indicating a UMA memory configuration.
Reserved	4	4	Reserved.
Resource ID Type [3 - ACPI Device]			
ACPI Hardware ID	8	0	_HID value of the ACPI Device corresponding to the Resource.
Resource ID Type [4 - PCI Device]			
PCIe Routing ID	4	0	The combination of a Segment Number, Bus Number, Device Number, and Function Number that uniquely identifies the PCI Express function or SIOV SDI.
Reserved	4	4	Reserved.
All Unspecified Resource ID Types			
Resource ID 1	8	0	Reserved.

Table 7. Resource ID 2

Field	Byte Length	Byte Offset	Description
Resource ID Type [2 - Memory-Side Cache]			
Cache Level	4	4	The Cache Level of the Memory Side Cache as identified by bits [7:4] of Cache Attributes structure from the corresponding Memory Side Cache Information Structure from HMAT.
Resource ID Type [3 - ACPI Device]			
ACPI Unique ID	4	0	_UID value of the ACPI Device corresponding to the Resource.
All Unspecified Resource ID Types			
Resource ID 2	4	0	Reserved.

Table 8. Resource Specific Data

Field	Byte Length	Byte Offset	Description
All Unspecified Resource Types			
	<i>For resource types specified by this specification, if a resource type is not identified below, then there is no Resource Specific Data defined for that resource type and the Length of the Resource Structure must be set to 20.</i>		
Resource Type [1 - Memory]			

Field	Byte Length	Byte Offset	Description
Bandwidth per Block	8	0	Indicates the bandwidth, in bytes per second, represented by each unit of the bandwidth block for this resource. If the value is 0, then the bandwidth per block is not provided.

2.1. RISC-V Memory Bandwidth QoS Controllers

2.1.1. Bandwidth Per Block Calculation

The Memory Bandwidth QoS controllers provide a generic means to control bandwidth in terms of blocks. The user may be interested in knowing exactly how much bandwidth a block entails, so that they can make informed decisions on how to size the per RCID bandwidth block configuration.

Given memory bandwidth will vary based on the type of memory connected to the system, the speed at which they are configured, the number of channels, interleaving conditions, etc., System BIOS or M-mode FW calculates the amount of Bandwidth pertaining to each controller's block unit. This is done by calculating the total bandwidth of all memory controllers within a memory region (proximity domain) and then dividing the total bandwidth by the number of bandwidth blocks that the controller governing that resource supports.

2.2. Shared Resource Configuration

In many system designs, a single logical resource may be managed by multiple QoS controllers. This occurs when the resource is physically distributed across multiple components, or when redundant controllers provide access to the same underlying resource. When multiple QoS controllers share responsibility for the same resource, they must be configured identically to ensure consistent behavior. Mismatched configurations across controllers managing the same resource can lead to unpredictable QoS enforcement and system behavior.

The resource association information provided in the RQSC table enables software to identify which controllers share responsibility for a common resource and must therefore maintain synchronized configurations.

2.2.1. Example: Memory Bandwidth Controllers in UMA and NUMA Configurations

System memory can be configured in one of two modes:

- **UMA (Uniform Memory Access):** All memory channels across different controllers are treated as a single unified memory range. Memory traffic is distributed equally among all controllers through interleaved addressing. In this configuration, memory affinity structures typically either omit memory descriptions entirely or describe all memory regions with the same proximity domain.
- **NUMA (Non-Uniform Memory Access):** Memory controllers are grouped into separate domains, with memory addresses partitioned among different channel groups. Within each NUMA node, traffic is still distributed equally among controllers through interleaved addressing. In this configuration, memory affinity structures describe memory regions with different proximity domains corresponding to their respective NUMA nodes.

In both configurations, when multiple memory bandwidth QoS controllers share the same proximity domain, their bandwidth reservation settings must be configured identically to ensure consistent bandwidth enforcement across all memory channels within that domain.

Chapter 3. Example ACPI Table Implementation

This chapter covers some system implementation examples.

3.1. Example 1: Single Socket System with 8 cores and 3 memory controllers

The diagram below shows a model of the SoC described in this example.

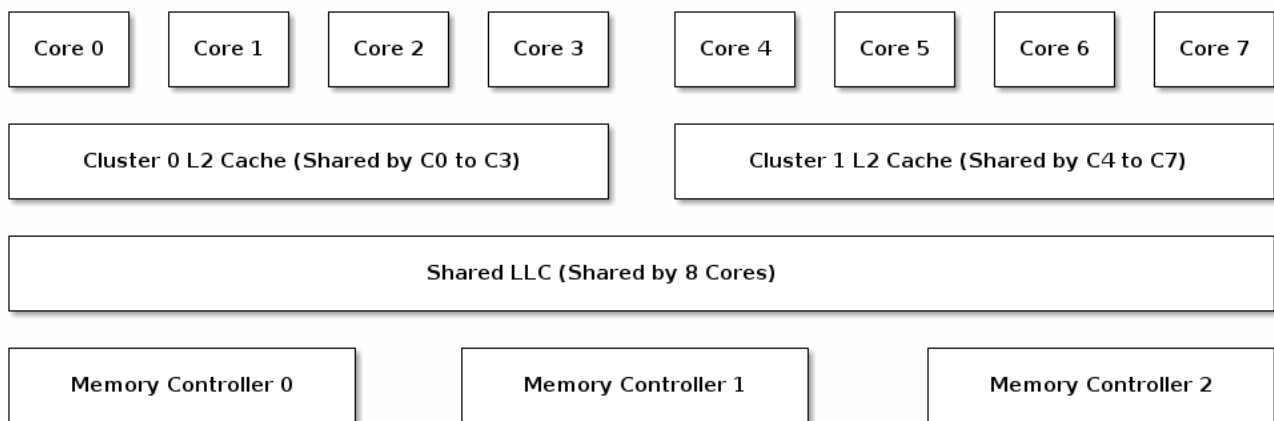


Figure 2. Single Socket System Example 1

In the example system above, Cluster 0 L2 cache is shared by 4 cores labeled Core 0 to 3. Cluster 1 L2 cache is shared by 4 cores labeled Core 4 to 7. Shared LLC (e.g. L3) is shared by all 8 cores. Shared LLC is connected to 3 memory controllers labeled 0 to 2. Each Memory Controller has 1 DDR Channel. The DDR Memory is configured in UMA mode with the same proximity domain for all memory channels.

The system implements the following Capacity and Memory Bandwidth QoS controllers.

- 2 L2 Cache Capacity QoS Controllers (one per cluster)
 - CBQRI located at **0x04821000** and **0x04822000**
- 1 LLC Cache Capacity QoS Controller
 - CBQRI located at **0x04823000**
- 3 Memory Bandwidth QoS Controllers (one per memory controller)
 - CBQRI located at **0x04828000**, **0x04829000** and **0x0482A000**

Globally all of the QoS Controllers implement 64 RCIDs and 256 MCIDs.

3.1.1. RQSC Table

```

Name(\RQSC, Package())
{
    "RQSC", // Signature
    0x00000148, // Total Length of RQSC Table (328 bytes)
}
  
```

```

0x01,          // Revision
0xFF,         // Checksum (placeholder, to be fixed)
"RIVOS ",     // OEMID
"RVOS  ",    // OEM Table ID
0x00000001,   // OEM Revision
"RVOS",      // Creator ID
0x00000001,   // Creator Revision
0x00000006,   // Number of QoS Controllers
Package()     // QoS Controller 1 - Cluster 0 L2 Cache Capacity QoS Controller
{
    0x00,      // Controller Type - Capacity
    0x00,      // Reserved
    44,        // Length
    Package() // Register Interface Address
    {
        0x00,          // System Memory Space
        0x00,          // Size of Register in bits (0)
        0x00,          // Register Offset (0)
        0x04,          // Access Size (DWORD)
        0x000000004821000, // Address
    },
    64,          // RCID Count
    256,         // MCID Count
    0x0000,     // Controller Flags
    0x0001,     // Number of Resources
    Package()   // Resource Structure - Cluster 0 L2 Cache
    {
        0x00,          // Resource Type (Cache)
        0x00,          // Reserved Byte
        20,           // Length (20 bytes)
        0x0000,       // Resource Flags
        0x00,          // Reserved Byte
        0x00,          // Resource ID Type (Processor Cache)
        0x0000000000000000, // Resource ID 1 (Cache ID from PPTT)
        0x00000000,   // Resource ID 2 (0)
    },
},
Package()     // QoS Controller 2 - Cluster 1 L2 Cache Capacity QoS Controller
{
    0x00,      // Controller Type - Capacity
    0x00,      // Reserved
    44,        // Length
    Package() // Register Interface Address
    {
        0x00,          // System Memory Space
        0x00,          // Size of Register in bits (0)
        0x00,          // Register Offset (0)
        0x04,          // Access Size (DWORD)
        0x000000004822000, // Address
    },
    64,          // RCID Count
    256,         // MCID Count
    0x0000,     // Controller Flags
    0x0001,     // Number of Resources
    Package()   // Resource Structure - Cluster 1 L2 Cache
    {
        0x00,          // Resource Type (Cache)
        0x00,          // Reserved Byte
        20,           // Length (20 bytes)
        0x0000,       // Resource Flags
        0x00,          // Reserved Byte
        0x00,          // Resource ID Type (Processor Cache)
        0x0000000000000001, // Resource ID 1 (Cache ID from PPTT)
        0x00000000,   // Resource ID 2 (0)
    },
},
Package()     // QoS Controller 3 - Shared LLC Cache Capacity QoS Controller

```

```

{
    0x00,          // Controller Type - Capacity
    0x00,          // Reserved
    44,           // Length
    Package()     // Register Interface Address
    {
        0x00,          // System Memory Space
        0x00,          // Size of Register in bits (0)
        0x00,          // Register Offset (0)
        0x04,          // Access Size (DWORD)
        0x0000000004823000, // Address
    },
    64,           // RCID Count
    256,          // MCID Count
    0x0000,       // Controller Flags
    0x0001,       // Number of Resources
    Package()     // Resource Structure - Shared LLC Cache
    {
        0x00,          // Resource Type (Cache)
        0x00,          // Reserved Byte
        20,          // Length (20 bytes)
        0x0000,       // Resource Flags
        0x00,          // Reserved Byte
        0x00,          // Resource ID Type (Processor Cache)
        0x0000000000000002, // Resource ID 1 (Cache ID from PPTT)
        0x00000000,   // Resource ID 2 (0)
    },
},
Package()        // QoS Controller 4 - Memory Controller 0 Bandwidth QoS Controller
{
    0x01,          // Controller Type - Bandwidth
    0x00,          // Reserved
    52,           // Length
    Package()     // Register Interface Address
    {
        0x00,          // System Memory Space
        0x00,          // Size of Register in bits (0)
        0x00,          // Register Offset (0)
        0x04,          // Access Size (DWORD)
        0x0000000004828000, // Address
    },
    64,           // RCID Count
    256,          // MCID Count
    0x0000,       // Controller Flags
    0x0001,       // Number of Resources
    Package()     // Resource Structure - Proximity Domain
    {
        0x01,          // Resource Type (Memory)
        0x00,          // Reserved Byte
        28,          // Length (28 bytes)
        0x0000,       // Resource Flags
        0x00,          // Reserved Byte
        0x01,          // Resource ID Type (Memory Range)
        0x0000000000000000, // Resource ID 1 (Proximity Domain from SRAT table for this memory)
        0x00000000,   // Resource ID 2 (0)
        0x0000000000000000, // Resource Specific Data (No bandwidth per block data reported)
    },
},
Package()        // QoS Controller 5 - Memory Controller 1 Bandwidth QoS Controller
{
    0x01,          // Controller Type - Bandwidth
    0x00,          // Reserved
    52,           // Length
    Package()     // Register Interface Address
    {
        0x00,          // System Memory Space
        0x00,          // Size of Register in bits (0)

```

```

        0x00,          // Register Offset (0)
        0x04,          // Access Size (DWORD)
        0x0000000004829000, // Address
    },
    64,              // RCID Count
    256,            // MCID Count
    0x0000,         // Controller Flags
    0x0001,         // Number of Resources
    Package()       // Resource Structure - Proximity Domain
    {
        0x01,          // Resource Type (Memory)
        0x00,          // Reserved Byte
        28,           // Length (28 bytes)
        0x0000,       // Resource Flags
        0x00,          // Reserved Byte
        0x01,          // Resource ID Type (Memory Range)
        0x0000000000000000, // Resource ID 1 (Proximity Domain from SRAT table for this memory)
        0x00000000,   // Resource ID 2 (0)
        0x0000000000000000, // Resource Specific Data (No bandwidth per block data reported)
    },
},
Package()         // QoS Controller 6 - Memory Controller 2 Bandwidth QoS Controller
{
    0x01,          // Controller Type - Bandwidth
    0x00,          // Reserved
    52,            // Length
    Package()       // Register Interface Address
    {
        0x00,          // System Memory Space
        0x00,          // Size of Register in bits (0)
        0x00,          // Register Offset (0)
        0x04,          // Access Size (DWORD)
        0x000000000482A000, // Address
    },
    64,              // RCID Count
    256,            // MCID Count
    0x0000,         // Controller Flags
    0x0001,         // Number of Resources
    Package()       // Resource Structure - Proximity Domain
    {
        0x01,          // Resource Type (Memory)
        0x00,          // Reserved Byte
        28,           // Length (28 bytes)
        0x0000,       // Resource Flags
        0x00,          // Reserved Byte
        0x01,          // Resource ID Type (Memory Range)
        0x0000000000000000, // Resource ID 1 (Proximity Domain from SRAT table for this memory)
        0x00000000,   // Resource ID 2 (0)
        0x0000000000000000, // Resource Specific Data (No bandwidth per block data reported)
    },
},
})

```

3.2. Example 2: Single Socket System with 8 cores and 4 memory controllers with NUMA enabled

The diagram below shows a model of the SoC described in this example.

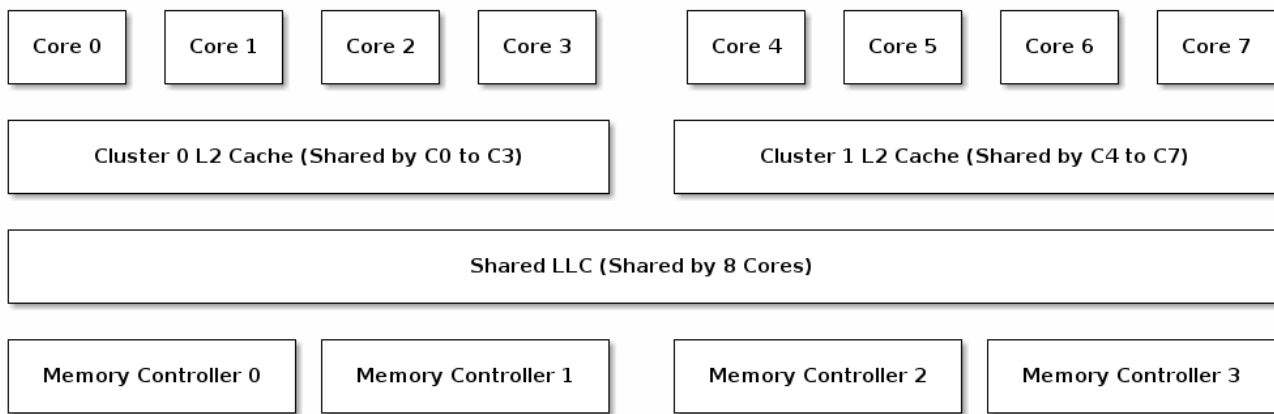


Figure 3. Single Socket System Example 2

In the example system above, Cluster 0 L2 cache is shared by 4 cores labeled Core 0 to 3. Cluster 1 L2 cache is shared by 4 cores labeled Core 4 to 7. Shared LLC (e.g. L3) is shared by all 8 cores. Shared LLC is connected to 4 memory controllers labeled 0 to 3. Each Memory Controller has 1 DDR Channel. The DDR Memory is configured in NUMA mode with 2 proximity domains where memory controllers 0 and 1 serve cores 0 to 3 and memory controllers 2 and 3 serve cores 4 to 7.

When configuring the QoS parameters for the memory QoS controllers, QoS controllers of memory controllers 0 and 1 must be configured with the same parameters and QoS controllers of memory controllers 2 and 3 must be configured with the same parameters.

The system implements the following Capacity and Memory Bandwidth QoS controllers.

- 2 L2 Cache Capacity QoS Controllers (one per cluster)
 - CBQRI located at **0x04821000** and **0x04822000**
- 1 LLC Cache Capacity QoS Controller
 - CBQRI located at **0x04823000**
- 4 Memory Bandwidth QoS Controllers (one per memory controller)
 - CBQRI located at **0x04828000**, **0x04829000**, **0x0482A000** and **0x0482B000**

Globally all of the QoS Controllers implement 64 RCIDs and 256 MCIDs.

3.2.1. RQSC Table

```
Name(\RQSC, Package())
{
  "RQSC",           // Signature
  0x0000017C,      // Total Length of RQSC Table (380 bytes)
  0x01,            // Revision
  0xFF,            // Checksum (placeholder, to be fixed up by tool)
  "RIVOS ",        // OEMID
  "RVOS ",         // OEM Table ID
  0x00000001,      // OEM Revision
  "RVOS",          // Creator ID
  0x00000001,      // Creator Revision
  0x00000007,      // Number of QoS Controllers
  Package()        // QoS Controller 1 - Cluster 0 L2 Cache Capacity QoS Controller
  {
    0x00,          // Controller Type - Capacity
```

```

0x00,          // Reserved
44,           // Length
Package()     // Register Interface Address
{
    0x00,          // System Memory Space
    0x00,          // Size of Register in bits (0)
    0x00,          // Register Offset (0)
    0x04,          // Access Size (DWORD)
    0x0000000004821000, // Address
},
64,           // RCID Count
256,          // MCID Count
0x0000,       // Controller Flags
0x0001,       // Number of Resources
Package()     // Resource Structure - Cluster 0 L2 Cache
{
    0x00,          // Resource Type (Cache)
    0x00,          // Reserved Byte
    20,           // Length (20 bytes)
    0x0000,       // Resource Flags
    0x00,          // Reserved Byte
    0x00,          // Resource ID Type (Processor Cache)
    0x0000000000000000, // Resource ID 1 (Cache ID from PPTT)
    0x00000000,   // Resource ID 2 (0)
},
},
Package()     // QoS Controller 2 - Cluster 1 L2 Cache Capacity QoS Controller
{
    0x00,          // Controller Type - Capacity
    0x00,          // Reserved
    44,           // Length
    Package()     // Register Interface Address
    {
        0x00,          // System Memory Space
        0x00,          // Size of Register in bits (0)
        0x00,          // Register Offset (0)
        0x04,          // Access Size (DWORD)
        0x0000000004822000, // Address
    },
    64,           // RCID Count
    256,          // MCID Count
    0x0000,       // Controller Flags
    0x0001,       // Number of Resources
    Package()     // Resource Structure - Cluster 1 L2 Cache
    {
        0x00,          // Resource Type (Cache)
        0x00,          // Reserved Byte
        20,           // Length (20 bytes)
        0x0000,       // Resource Flags
        0x00,          // Reserved Byte
        0x00,          // Resource ID Type (Processor Cache)
        0x0000000000000001, // Resource ID 1 (Cache ID from PPTT)
        0x00000000,   // Resource ID 2 (0)
    },
},
Package()     // QoS Controller 3 - Shared LLC Cache Capacity QoS Controller
{
    0x00,          // Controller Type - Capacity
    0x00,          // Reserved
    44,           // Length
    Package()     // Register Interface Address
    {
        0x00,          // System Memory Space
        0x00,          // Size of Register in bits (0)
        0x00,          // Register Offset (0)
        0x04,          // Access Size (DWORD)
        0x0000000004823000, // Address
    }
}

```

```

    },
    64,           // RCID Count
    256,         // MCID Count
    0x0000,     // Controller Flags
    0x0001,     // Number of Resources
    Package()   // Resource Structure - Shared LLC Cache
    {
        0x00,           // Resource Type (Cache)
        0x00,           // Reserved Byte
        20,           // Length (20 bytes)
        0x0000,       // Resource Flags
        0x00,           // Reserved Byte
        0x00,           // Resource ID Type (Processor Cache)
        0x0000000000000002, // Resource ID 1 (Cache ID from PPTT)
        0x00000000,   // Resource ID 2 (0)
    },
},
Package()      // QoS Controller 4 - Memory Controller 0 Bandwidth QoS Controller
{
    0x01,       // Controller Type - Bandwidth
    0x00,       // Reserved
    52,         // Length
    Package()   // Register Interface Address
    {
        0x00,           // System Memory Space
        0x00,           // Size of Register in bits (0)
        0x00,           // Register Offset (0)
        0x04,           // Access Size (DWORD)
        0x0000000004828000, // Address
    },
    64,           // RCID Count
    256,         // MCID Count
    0x0000,     // Controller Flags
    0x0001,     // Number of Resources
    Package()   // Resource Structure - Proximity Domain
    {
        0x01,           // Resource Type (Memory)
        0x00,           // Reserved Byte
        28,           // Length (28 bytes)
        0x0000,       // Resource Flags
        0x00,           // Reserved Byte
        0x01,           // Resource ID Type (Memory Range)
        0x0000000000000000, // Resource ID 1 (Proximity Domain from SRAT table for this memory)
        0x00000000,   // Resource ID 2 (0)
        0x0000000000000000, // Resource Specific Data (No bandwidth per block data reported)
    },
},
Package()      // QoS Controller 5 - Memory Controller 1 Bandwidth QoS Controller
{
    0x01,       // Controller Type - Bandwidth
    0x00,       // Reserved
    52,         // Length
    Package()   // Register Interface Address
    {
        0x00,           // System Memory Space
        0x00,           // Size of Register in bits (0)
        0x00,           // Register Offset (0)
        0x04,           // Access Size (DWORD)
        0x0000000004829000, // Address
    },
    64,           // RCID Count
    256,         // MCID Count
    0x0000,     // Controller Flags
    0x0001,     // Number of Resources
    Package()   // Resource Structure - Proximity Domain
    {
        0x01,           // Resource Type (Memory)

```

```

    0x00,          // Reserved Byte
    28,           // Length (28 bytes)
    0x0000,      // Resource Flags
    0x00,        // Reserved Byte
    0x01,        // Resource ID Type (Memory Range)
    0x0000000000000000, // Resource ID 1 (Proximity Domain from SRAT table for this memory)
    0x00000000,  // Resource ID 2 (0)
    0x0000000000000000, // Resource Specific Data (No bandwidth per block data reported)
  },
},
Package()      // QoS Controller 6 - Memory Controller 2 Bandwidth QoS Controller
{
  0x01,        // Controller Type - Bandwidth
  0x00,        // Reserved
  52,         // Length
  Package()    // Register Interface Address
  {
    0x00,      // System Memory Space
    0x00,      // Size of Register in bits (0)
    0x00,      // Register Offset (0)
    0x04,      // Access Size (DWORD)
    0x000000000482A000, // Address
  },
  64,         // RCID Count
  256,        // MCID Count
  0x0000,     // Controller Flags
  0x0001,     // Number of Resources
  Package()   // Resource Structure - Proximity Domain
  {
    0x01,     // Resource Type (Memory)
    0x00,     // Reserved Byte
    28,       // Length (28 bytes)
    0x0000,   // Resource Flags
    0x00,     // Reserved Byte
    0x01,     // Resource ID Type (Memory Range)
    0x0000000000000001, // Resource ID 1 (Proximity Domain from SRAT table for this memory)
    0x00000000, // Resource ID 2 (0)
    0x0000000000000000, // Resource Specific Data (No bandwidth per block data reported)
  },
},
Package()     // QoS Controller 7 - Memory Controller 3 Bandwidth QoS Controller
{
  0x01,        // Controller Type - Bandwidth
  0x00,        // Reserved
  52,         // Length
  Package()    // Register Interface Address
  {
    0x00,      // System Memory Space
    0x00,      // Size of Register in bits (0)
    0x00,      // Register Offset (0)
    0x04,      // Access Size (DWORD)
    0x000000000482B000, // Address
  },
  64,         // RCID Count
  256,        // MCID Count
  0x0000,     // Controller Flags
  0x0001,     // Number of Resources
  Package()   // Resource Structure - Proximity Domain
  {
    0x01,     // Resource Type (Memory)
    0x00,     // Reserved Byte
    28,       // Length (28 bytes)
    0x0000,   // Resource Flags
    0x00,     // Reserved Byte
    0x01,     // Resource ID Type (Memory Range)
    0x0000000000000001, // Resource ID 1 (Proximity Domain from SRAT table for this memory)
    0x00000000, // Resource ID 2 (0)
  }
}

```

```
        0x0000000000000000, // Resource Specific Data (No bandwidth per block data reported)
    },
},
})
```

Bibliography

[1] “Advanced Configuration and Power Interface Specification.” [Online]. Available: uefi.org/specs/ACPI/6.6/.

[2] “RISC-V Capacity and Bandwidth Controller QoS Register Interface.” [Online]. Available: github.com/riscv-non-isa/riscv-cbqri.